

REMARKS

Claims 1, 33, 42, 50, 52, 57, 76, 112, 118, 130 and 146 have been amended. Claims 52 and 53 have been withdrawn. No new matter has been included. Claims 1-51 and 54-172 are pending in the present application. Applicant notes that the claim amendments will affect the "provisional" double-patenting rejections, which are discussed below.

Claims 1, 33, 50, 52, 53 and 146 stand objected to based on certain informalities. Applicant has amended these claims to include the appropriate corrections. Accordingly, Applicant respectfully requests that the objection be withdrawn.

Claim 118 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has amended claim 118 accordingly. Applicant respectfully requests that this rejection be withdrawn.

The following section of the remarks address the double-patenting rejections which are mostly "provisional" rejections. In addition to the specific remarks below, Applicant would note more generally that there have been substantive amendments to some of the claims currently "provisionally" rejected and as a result, the double-patenting rejection would no longer apply.

Claims 1-88 and 112-129 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 76-87 of copending Application No. 10/819315. Application No. 10/819315 is pending at this time and its claims, as well as those in the present application, are

subject to change, thus Applicant does not respond to this rejection at this time. However, Applicant reserves the right to respond to the rejection if necessary when it is no longer a "provisional" rejection.

Claims 1-172 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 30-137 of copending Application No. 10/120521 in view of Campbell et al. (U.S. Patent No. 6,813,178)("Campbell"). Application No. 10/120521 is pending at this time and its claims, as well as these in the present application, are subject to change, thus Applicant does not respond to this rejection at this time. However, Applicant reserves the right to respond to the rejection if necessary when it is no longer a "provisional" rejection.

Claims 130-147 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over allowed and renumbered claim 89 of copending Application No. 10/230201 in view of Campbell. This provisional rejection is respectfully traversed. Application No. 10/230201 is now U.S. Patent No. 6,867,996 (the '996 patent). Applicant notes that claim 89 of the '996 patent (Application No. 10/230201) has been allowed and thus, responds to the provisional rejection.

The doctrine of double patenting seeks to prevent the unjustified extension of patent exclusivity beyond the term of a patent. Double patenting results when the right to exclude granted by a first patent is unjustly extended by the grant of a later issued patent or patents. M.P.E.P. § 804. The present claims must be obvious variations of allowed or patented claims for the rejection to be proper.

Claim 130 recites a processor-based system comprising "a memory circuit connected to said processor, said memory circuit including a resistance variable

memory element comprising a plurality of layers configured for retaining stored data as a resistance value and for exhibiting a resistance change in response to an applied programming voltage, said plurality of layers comprising at least one metal-containing layer, at least one silver layer in contact with said at least one metal-containing layer, at least one chalcogenide glass layer, at least one other glass layer, said metal-containing layer and said silver layer being provided between said at least one chalcogenide glass layer and said at least one other glass layer." On the other hand, claim 89 of the '996 patent depends from claim 82, and recites "a resistance variable memory element comprising a PCRAM stack including amorphous semiconducting glass layers separated by a layer of silver-containing material."

The present invention recites "at least one metal-containing layer, [and] at least one silver layer in contact with said at least one metal-containing layer," whereas the '996 patent only recites "a layer of silver-containing material" between the glass layers. The present invention and the '996 patent do not recite the same limitations, and present claimed structure is not obvious over claim 89 of the '996 patent. Moreover, Campbell relates to a chalcogenide constant current device, and not a resistance variable memory element. Consequently, it would not have been an obvious variation of claim 89 of the '966 patent to include "at least one metal-containing layer, [and] at least one silver layer" within a resistance variable memory element, as claimed in present application claims 130-147.

Accordingly, Applicant respectfully requests that the double-patenting rejection be withdrawn and the claims allowed.

Claims 112-129 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 71 of

compending Application No. 10/800707 in view of Campbell. Application No. 10/800707 is pending at this time and its claims, as well as the claims of the present application, are subject to change, thus Applicant does not respond to this rejection at this time. However, Applicant reserves the right to respond to the rejection if necessary when it is no longer a provisional rejection.

Claims 1-56 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 30 of compending Application No. 10/410567 in view of Campbell. Application No. 10/410567 is pending at this time and its claims, as well as those of the present application, are subject to change, thus Applicant does not respond to this rejection at this time. However, Applicant reserves the right to respond to the rejection if necessary when it is no longer a "provisional" rejection.

Claims 1-5, 9-11, 15-21, 23, 25-27, 29-31, 33, 34, 38-42, 46, 47, 49-55, 57-60, 64, 68, 70-74, 76-80, 84-87, 112-120, 124, 125, 127, 128, 130-135, 137, 139, 140, 144 and 145-147 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Campbell. The rejection is respectfully traversed.

Claim 1 recites a resistance variable memory element comprising "a plurality of layers configured for retaining stored data and exhibiting a resistance change in response to an applied voltage." Campbell relates to a chalcogenide constant current device, and not a resistance variable memory element. Campbell fails to disclose a memory element comprising "a plurality of layers configured for retaining stored data as a resistance value and for exhibiting a resistance change in response to an applied programming voltage."

Campbell and the present invention do have similar structures. However, Campbell permanently changes the internal structure of the device. Campbell applies a negative electrical pulse of an absolute amplitude greater than the erase potential of the device in order to have the device exhibit constant current behavior. The negative electrical pulse is significantly more negative than the erase potential that is applied to a memory element. As a result, the structure's electrical behavior is altered and constant current source behavior is exhibited rather than memory behavior. (col. 6, lines 37-63). The devices fabricated in Campbell's manner are permanently converted to constant current operation devices. (col. 7, lines 16-19). Accordingly, the Campbell structure and that of the present invention are structurally different.

Consequently, Campbell does not disclose the limitations of the claim 1 invention. Claims 2-5, 9-11, 15-21, 23, 25-27 and 29-31 depend from claim 1 and should be allowable along with claim 1.

Claim 33 recites a resistance variable memory element comprising "a plurality of layers configured for retaining stored data as a resistance value and for exhibiting a resistance change in response to an applied programming voltage." As set forth above, Campbell does not disclose a memory element. Thus, Campbell fails to disclose the limitations of claim 33. Claims 34, 38-42, 46, 47 and 49-55 depend from claim 33 and should be allowable along with claim 33.

Claim 57 recites a memory element comprising "a plurality of layers configured for retaining stored data as a resistance value and for exhibiting a resistance change in response to an applied programming voltage." Campbell discloses no such limitation. For at least the reasons set forth above, Campbell fails to disclose a memory element "for retaining stored data as a resistance value and for exhibiting a resistance

change in response to an applied programming voltage." Consequently, Campbell does not disclose the limitations of claim 57. Claims 58-60, 64, 68 and 70-74 depend from claim 57 and should be allowable along with claim 57.

Claim 76 recites a chalcogenide glass stack comprising "a plurality of layers configured for retaining stored data as a resistance value and for exhibiting a resistance change in response to an applied programming voltage." As set forth above, Campbell does not disclose such a limitation. Thus, Campbell fails to disclose the limitations of claim 76. Claims 77-80 and 84-87 depend from claim 76 and should be allowable along with claim 76.

Claim 112 recites a method of forming a resistance variable memory element comprising "a plurality of layers configured for retaining stored data as a resistance value and for exhibiting a resistance change in response to an applied programming voltage." As set forth above, Campbell does not disclose such a limitation. Thus, Campbell fails to disclose the limitations of claim 112. Claims 113-120, 124, 125, 127 and 128 depend from claim 112 and should be allowable along with claim 112.

Claim 130 recites a processor-based system "including a resistance variable memory element comprising a plurality of layers configured for retaining stored data as a resistance value and for exhibiting a resistance change in response to an applied programming voltage." As set forth above, Campbell does not disclose such a limitation. Thus, Campbell fails to disclose the limitations of claim 130. Claims 131-135, 137, 139, 140, 144 and 145-147 depend from claim 130 and should be allowable along with claim 130.

Accordingly, Campbell fails to establish a prima facie showing of anticipation under § 102(e). Therefore, Applicant respectfully requests that the rejection be withdrawn and the claims allowed.

Claims 1-3, 9, 10, 15, 23, 25, 26, 30, 32, 130-135, 137, 139 and 144-146 stand rejected under 35 U.S.C. § 102(a) as being anticipated by Moore (U.S. Publication No. 2003/0038301)("Moore"). The rejection is respectfully traversed.

Claim 1 recites "a resistance variable memory element," formed of specific layers. Moore discloses two individual memory elements that are stacked one over the other with a common anode between them to form an upper and lower memory cell pair. Moore at page 1, paragraph 15. Each of Moore's memory elements includes a substrate, an insulator layer, a chalcogenide glass layer, and another insulator layer. Moore does not disclose "a memory cell" having the construction of "at least one metal-containing layer, at least one silver layer in contact with said at least one metal-containing layer, at least one chalcogenide glass layer, at least one other glass layer, said metal-containing layer and said silver layer being provided between said at least one chalcogenide glass layer and said at least one other glass layer." One can not consider the layers of two different memory cells in Moore as layers of the "memory cell" as claimed. Thus, Moore does not disclose the limitations of the claim 1 invention. Claims 2, 3, 9, 10, 15, 23, 25, 26, 30 and 32 depend from claim 1 and should be allowable along with claim 1.

Claim 130 recites "a memory circuit connected to said processor, said memory circuit including a resistance variable memory element comprising a plurality of layers configured for retaining stored data as a resistance value and for exhibiting a resistance change in response to an applied programming voltage, said plurality of

layers comprising at least one metal-containing layer, at least one silver layer in contact with said at least one metal-containing layer, at least one chalcogenide glass layer, at least one other glass layer, said metal-containing layer and said silver layer being provided between said at least one chalcogenide glass layer and said at least one other glass layer." Again, Moore fails to disclose such a memory cell construction. Claims 131-135, 137, 139 and 144-146 depend from claim 130 and should be allowable along with claim 130.

For at least these reasons, Moore fails to make a prima facie showing of anticipation. Accordingly, Applicant respectfully submits that the § 102(a) rejection should be withdrawn and the claims allowed.

Claims 1, 22, 130 and 138 stand rejected under 35 U.S.C. § 102(a) as being anticipated by Moore based on, as referred to in the Office Action, an alternate interpretation. The rejection is respectfully traversed.

Claim 1 recites a resistance variable memory element comprising: "at least one chalcogenide glass layer, at least one metal-containing layer, at least one silver layer provided adjacent to said metal-containing layer, and at least one other glass layer, said at least one metal-containing layer and said at least one silver layer being provided between at least one chalcogenide glass layer and said at least one other glass layer." Moore fails to disclose a memory cell having this construction. Moore discloses the use of two memory elements stacked one over the other with a common anode between them to form an upper and lower cell pair. In Moore, the two memory elements can be accessed separately to store two bits of data.

The Office Action is disregarding the plain teachings of Moore by combining layers of two different memory elements in an attempt to form the recited memory

element. Moore does not disclose, teach or suggest such a combination. Each of Moore's separate memory elements includes a substrate, an insulator layer, a chalcogenide glass layer, and another insulator layer. The present claimed memory element comprises "at least one chalcogenide glass layer, at least one metal-containing layer, at least one silver layer provided adjacent to said metal-containing layer, and at least one other glass layer." The Office Action is articulating a teaching of Moore which is simply not disclosed by Moore.

Moreover, Moore discloses layers 105 and 129, which are each a chalcogenide glass material and can be formed as Ag/Ge₃Se₇, and a silver layer 110. Moore at col. 2, lines 45-53; col. 3, lines 1-8. The Examiner asserts that Moore's layer 105 is amorphous and therefore can be considered to consist of multiple layers. However, claim 1 recites two distinct glass layers, "at least one chalcogenide layer" and "at least one other glass layer." Thus, Moore fails to disclose all the limitations of claim 1. Claim 22 depends from claim 1 and should be allowable along with claim 1.

Claim 130 recites "a memory circuit connected to said processor, said memory circuit including a resistance variable memory element comprising a plurality of layers configured for retaining stored data as a resistance value and for exhibiting a resistance change in response to an applied programming voltage, said plurality of layers comprising at least one metal-containing layer, at least one silver layer in contact with said at least one metal-containing layer, at least one chalcogenide glass layer, at least one other glass layer, said metal-containing layer and said silver layer being provided between said at least one chalcogenide glass layer and said at least one other glass layer." For at least the reasons set forth above, Moore does not disclose the memory element of the present invention having two distinct glass layers. Thus, Moore

does not disclose the limitations of the claim 130 invention. Claim 138 depends from claim 130 and should be allowable along with claim 130.

Accordingly, Applicant respectfully submits that Moore does not establish a prima facie case of anticipation. Thus, Applicant respectfully requests that the § 102(a) rejection be withdrawn and the claims allowed.

Claims 16-21, 27, 28, 31 and 147 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Moore. The rejection is respectfully traversed.

As provided by 35 U.S.C. § 103(c), Moore is not permitted to preclude patentability under 35 U.S.C. § 103(a). The subject matter of Moore and the claimed invention were, at the time the invention was made, subject to an obligation of assignment to the same entity: Micron Technology, Inc. The assignment for the present application was recorded in the PTO on July 21, 2003, on Reel 014316, Frame 0476. The Assignee of Moore is shown on the attached copy of the Notice of Recordation of Assignment Document. Therefore, 35 U.S.C. § 103(c) applies and Applicants respectfully request withdrawal of this rejection.

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In view of the above amendment, Applicant believes the pending application is in condition for allowance.

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